REGULATOR WITH VARIABLE CAPACITOR FOR STABILITY COMPENSATION

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FIELD OF THE INVENTION

[0001] The present invention relates to voltage regulators and in particular to voltage regulators for variable current loads.

BACKGROUND

[0002] There is an increasing need for low-voltage, low drop out regulators due to the growing demand in portable electronics, which require low power and low cost system-on-chip designs.

[0003] Fig. 1 illustrates a conventional low drop PMOS output regulator 10 that is composed of two gain stages with a negative feedback. The first stage is an error amplifier 12 with a trans-conductance of gm_1. Feedback is provided to the amplifier 12 from a voltage divider with resistors 14 and 16. The amplifier 12 receives the input voltage and a reference voltage Vref on the negative input terminal and the feedback on the positive input terminal. The output stage is a PMOS transistor 18, which has a transconductance of gm_2. The output stage of regulator 10 has a common source configuration. The gate of the transistor 18 is coupled to the Vout through a compensation capacitor 20. The load of regulator 10 is illustrated as current source I_L, and resistor R_L, while capacitor C_L is a load capacitor.

[0004] In order to obtain enough phase margin for stability of the closed loop transfer function with a constant load, the design should obey the following:

$$\frac{1}{3} = \frac{gm_1 * C_L}{gm_2 * C_C} \qquad \text{eq. 1}$$

where C_L is the total load capacitance, and C_C is the compensation capacitance from capacitor 20. In order to obtain more phase margin, a series resistor, $R>1/gm_2$, can be inserted between capacitor 20 and the Vout. Such a series resistor results in more closed loop phase margin for better stability.

[0005] The design of a regulator 10 that meets equation 1 is not difficult where there is a constant and static current load. Unfortunately, where a variable and dynamic current load is present, regulator 10 is inadequate. Thus, for an on-chip load that generates a very large dynamic spike current, such as that might be found in field programmable gate arrays (FPGAs), the variable dynamic load current will generate a large amount of output voltage noise through the output impedance of the regulator. For example, where the current load is 1.5A p-p, and the DC impedance of the regulator output is 1ohm, the resulting noise will be 1.5V p-p, e.g., Vout(noise) = 1.5Ap-p * 1ohm =1.5Vp-p. If the regulator output is driving a large variable dynamic spike current load, the loop stability through a frequency compensation because particularly difficult to manage.

[0006] Accordingly, an improved regulator is needed, particularly for applications that may have dynamic and variable currents, such as in field programmable gate arrays (FPGAs) where the current load depends on the end user's program.

SUMMARY

[0007] In accordance with an embodiment of the present invention, a regulator includes a variable compensation capacitor, which enables the regulator to drive a large variable dynamic current load. Accordingly, the regulator is particularly useful in programmable devices, such as FPGAs in which the current load varies based upon the end user's desired circuit. A plurality of regulators may be used to drive the same load within a programmable device.

[0008] In one embodiment, an apparatus includes a regulator having a first amplifier with a first input terminal coupled to a reference terminal of the regulator to receive a reference voltage. The regulator also includes a second amplifier that has a first terminal coupled to the output terminal of the first amplifier. The second amplifier has a second terminal that receives the input voltage and a third terminal that is coupled to the regulator's output terminal. The second amplifier's third terminal is also coupled to a second input terminal of the first amplifier. The regulator further includes a variable capacitor that is disposed between the output terminal of the first amplifier and the third terminal of the second amplifier. In one embodiment, the variable capacitor may be a transistor with its gate coupled to the output

terminal of the first amplifier and the drain and source both coupled to the second terminal of the second amplifier. There may be a transistor disposed between the second terminal of the second amplifier and the variable capacitor. In another embodiment, a plurality of regulators has output terminals coupled together and are all included on a single integrated circuit.

[0009] In another aspect of the present invention, a method of regulating a voltage includes providing an input voltage and providing a reference voltage. A first stage output voltage is generated based on the reference voltage and a feedback voltage. To produce a regulated output voltage, the amplification of an input voltage is controlled based on the first stage output voltage. Instabilities in the input voltage are compensated for using a variable capacitance between the first stage output voltage and a second voltage that is based on the regulated output voltage. The second voltages may be the regulated output voltage minus a gate source voltage of a transistor. The feedback voltage may be produced by dividing the regulated output voltage. In one embodiment, a plurality of regulated output voltages a produced and combined. The combined regulated output voltages are then provided to a load.

[0010] Another aspect of the present invention is an integrated circuit that includes a plurality of regulators for receiving in input voltage and providing a plurality of regulated output voltages. The integrated circuit includes a programmable portion of the integrated circuit, wherein each of the plurality of regulators is approximately equidistance from the programmable portion within the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 illustrates a conventional low drop PMOS output regulator that is composed of two gain stages with a negative feedback.

[0012] Fig. 2 illustrates a regulator in accordance with an embodiment of the present invention.

[0013] Fig. 3 illustrates the variable capacitor used in one embodiment of the present invention.

[0014] Fig. 4 illustrates the capacitance of variable capacitor where the X-axis represents the voltage (V_G-V_C) and the Y-axis represents the capacitance in pF.

[0015] Fig. 5 illustrates a simulation result of the phase margin versus the load current of the regulator.

[0016] Fig. 6 schematically illustrates an on-chip regulator topology in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION

[0017] Fig. 2 illustrates a regulator 100 in accordance with an embodiment of the present invention. Regulator 100 may be, e.g., an FPGA core cell power supply that is built on the chip and is capable of handling a large variable dynamic current, e.g., up to 1.5A p-p, from the user's programmed portion of the FPGA. As can be seen in Fig. 2, the output load is modeled with a variable current I_L and resistance R_L. The output stage of regulator 100 is a PMOS transistor 102 in a common source configuration.

[0018] The regulator 100 includes a negative feedback system that provides a regulator output voltage with low output impedance, high input impedance, high open loop gain and a sufficient loop stability that the voltage output can be represented by the following equation with little or no error factors.

$$Vout = Vref\left(1 + \frac{R_{106}}{R_{108}}\right) \qquad \text{eq. 2}$$

[0019] As illustrated in Fig. 2, the regulator 100 includes an error amplifier 104 that receives feedback at the positive input terminal from the voltage divider composed of resistors 106 and 108. The transconductance of amplifier 104 will be referred to herein as gm_1 while the transconductance of transistor 102 will be referred to herein as gm_2. The amplifier 104 receives an input voltage from Vin and a reference voltage Vref on the negative input terminal. An NMOS transistor 110 has its gate coupled to the output voltage Vout and its source coupled to the output terminal of the amplifier 104 and the gate of the PMOS transistor 102 via a variable compensation capacitor 112. The source of the transistor 110 is also coupled to ground through a current source 114. The drain of transistor 110 is coupled to Vin.

[0020] Advantageously, the use of the variable capacitor 112 permits a constant ratio in the denominator of equation 1, e.g., $3=gm_2*C_C$, where the value C_c represents the capacitance of the variable compensation capacitor 112 in Fig. 2. A constant ratio in the denominator (and in the numerator) of equation 1, advantageously provides good loop stability.

[0021] The total output drive current of regulator 100 is represented as follows:

$$I_{102} = Iq + I_L \qquad \text{eq. 3}$$

where $Iq = Vout/(R_{106}+R_{108})$ and I_L is the variable load current, e.g., as provided by the programmed FPGA. The voltages at nodes V_G and V_C in Fig. 2 can be represented as:

$$V_G = Vin - V_{GS102} \qquad \text{eq. 4}$$

$$V_C = Vout - V_{GS110} \qquad \text{eq. 5}$$

where V_{GS102} and V_{GS110} is the gate source voltages of transistors 102 and 110, respectively. If the output drive current I_{102} is approximately equal to the variable load current I_L, the voltage V_{GS102} can be represented as follows:

$$V_{GS102} = \sqrt{\frac{2I_L}{K_{102}}} + Vth_{102} \qquad \text{eq. 6}$$

where $Iq << I_L$ and $K_{102} = \mu_{102}*Cox*(W/L)_{102}$, is the trans-conductance parameter of transistor 102, μ_{102} is the surface mobility of the channel for transistor 102, Cox is the capacitance per unit area of the gate oxide and $(W/L)_{102}$ is the width and length of the channel for transistor 102, and the term Vth_{102} is the threshold voltage for transistor 102.

[0022] The transconductance gm_2 for transistor 102 may be written as follows:

$$gm_2 = \sqrt{2 * K_{102} * I_L}\ . \qquad \text{eq. 7}$$

Further, the capacitance C_C of the variable compensation capacitor 112 can be written as:

$$C_C = Cox\left(W/L\right)*\left(V_G - V_C\right)$$
$$= Cox\left(W/L\right)*\left(Vin - V_{GS102} - V_C\right) \qquad \text{eq. 8}$$
$$= Cox\left(W/L\right)*\left(Vin - \sqrt{\frac{2I_L}{K_{102}}} + Vth_{102} - V_C\right).$$

[0023] Fig. 3 illustrates one embodiment of the variable capacitor 112 as a PMOS transistor 112a with the source coupled to the drain. Fig. 4 illustrates the capacitance of variable capacitor 112 where the X-axis represents the voltage (V_G-V_C) and the Y-axis represents the capacitance in pF.

[0024] With the use of the variable capacitor 112, the denominator term in equation 1, $3=gm_2*C_C$, is maintained over a variation in the load current I_L, since the transconductance gm_2 and the capacitance C_C have inverse characteristics as shown in equations 7 and 8 above, i.e., where gm_2 is related to $+\sqrt{I_L}$ and C_C is related to $-\sqrt{I_L}$. Accordingly, the phase margin of the regulator 100 will not worsen over variation in the load current I_L.

[0025] Fig. 5 illustrates a simulation result of the phase margin versus the load current. The broken line 214 represents the phase margin for a conventional regulator 10 with a constant compensation capacitor 20, while the solid line 212 represents the phase margin for regulator 100 with variable capacitor 112 based on the reverse bias Section-II MOS capacitor characteristic curve from Fig. 4. As can be seen, the variable capacitor 112 provides an approximately constant phase margin 212 for load current variations up to 300mA, while the phase margin 214 for the constant capacitor 20 significantly decreases over the same range.

[0026] The reference voltage Vref should be a band-gap reference voltage. The reference voltage Vref is provided by a constant current source 152 and a resistor 154 in series with a pnp bipolar transistor 156 with its base tied to ground. The current driving configuration shown in Fig. 2 can be used to drive multiple junctions over a long distance, wide die area with a single constant current generator.

[0027] Fig. 6 schematically illustrates an on-chip regulator topology in accordance with another embodiment of the present invention. The topology of Fig. 6 advantageously provides on-chip regulator biasing over a large area, e.g., 8mm x 8mm. Fig. 6 shows a chip 300, such as

an FPGA or other semiconductor device, with a variable load 301 and a plurality of separate regulators 302A, 302B, 302C, and 302D, collectively referred to herein sometimes as regulators 302. The variable load 301 may be, e.g., a programmable portion of an integrated circuit. The regulators 302 are located in different sections of the chip 300, indicated by the broken lines. By way of example, four regulators 302 are shown in Fig. 6, with each regulator placed in a different quadrant. If desired, however, additional regulators may be located symmetrically within chip 300, i.e., approximately equidistant from the programmable portion, i.e., the load 301, of the chip. Thus, the current driving density of the device is reduced, which reduces thermal degradation of contact and metal layers thereby securing long-term reliability of the device.

[0028] In one embodiment, the input voltage Vin_A, Vin_B, Vin_C, and Vin_D to the plurality of regulators 302A, 302B, 302C, and 302D, respectively, are the same input voltages and can be supplied from different pads on the chip 300 or from the same pad. The reference voltages $Vref_A$, $Vref_B$, $Vref_C$, and $Vref_D$ for the plurality of regulators 302A, 302B, 302C, and 302D, respectively, are the same band-gap reference voltages with the same constant current bias, Ir_A, Ir_B, Ir_C, and Ir_D., which is generated by the a common bias circuit block, e.g., illustrated in Fig. 2.

[0029] Each of the regulators 302 is the same as regulator 100 shown in Fig. 2. The use of four regulators 302, advantageously, reduces the output-driving requirement of the any single regulator by one quarter. Thus, the size of the output transistor 102 and the load capacitor C_L, shown in Fig. 2, may be reduced by one quarter. By way of example, with four regulators 302 used, the output transistor 102 (from Fig. 2) may have a size W/L of 8000/0.3 and the C_L may be 1225pF. If only one regulator were used, the transistor size would be W/L 32000/0.3, and the C_L would be 4900pF. By coupling all the regulators 302 to the variable load 301, as well as placing the regulators 302 approximately equidistant to the variable load 301, the parasitic components of the layout connection is reduced.

[0030] The output voltages $Vout_A$, $Vout_B$, $Vout_C$, and $Vout_D$ from the plurality of regulators 302A, 302B, 302C, and 302D, respectively, are combined and provided as a single output voltage Vout to the variable load 301. The output voltage Vout is the average of the output voltages from each of the regulators 302, i.e.,

$$Vout = \frac{1}{4}\left(Vout_A + Vout_B + Vout_C + Vout_D\right). \qquad \text{eq. 9}$$

Similarly, the output voltage noise will also be the average of the voltage noise from each regulator.

[0031] Although the present invention is illustrated in connection with specific embodiments for instructional purposes, the present invention is not limited thereto. Various adaptations and modifications may be made without departing from the scope of the invention. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.